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EXAMINER	
VU, QUANG D	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/083,756	Applicant(s) KIM ET AL.	
	Examiner Quang D. Vu	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 24 November 2004.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-15,17,18,20-22 and 24-26 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-15,17,18,20-22 and 24-26 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3 and 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 4,804,633 to Macelwee et al. in view of US Patent No. 5,643,822 to Furukawa et al. and US Patent No. 6,231,673 to Maeda.

Regarding claim 1, Macelwee et al. (figure 4) teach a method for forming an oxide layer having a first thickness (the thickness of layer [30] and [32] is about 3100 angstroms) in an integrated circuit device process, comprising:

forming the pad oxide layer (thermal oxide [32]) having a second thickness (thickness of layer [32] is about 100 angstroms) thinner than the first thickness using a thermal oxidation method on a surface of a semiconductor substrate (10); and

forming an oxide layer (30) having a third thickness (thickness of layer [30] is about 3000 angstroms) substantially equal to a difference between the first thickness (3100 angstroms) and the second directly thickness (100 angstroms) on the thermal oxide layer (32).

Macelwee et al. differ from the claimed invention by not showing forming a CVD oxide layer. However, Furukawa et al. teach forming a CVD oxide layer (column 3, lines 48-50). Therefore, it would have been obvious to one having ordinary skill in the art at the time the

invention was made to incorporate the teaching of Furukawa et al. into the device taught by Macelwee et al. in order to improve the liability of the oxide layer.

The combined device differs in not showing forming a thermal oxide layer and a CVD oxide layer in the same CVD apparatus. However, Maeda (figure 25) teaches conducting processing such as heat treatment, thermal oxidation, and CVD processing (column 15, lines 51-55), a single apparatus, which reads on a CVD apparatus. It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching Furukawa et al. into the device taught by Macelwee et al. and Furukawa et al. in order to reduce the processing time and contamination.

Regarding claim 2, the combined device shows the thermal oxide (Macelwee et al.; 32) is formed to a thickness of approximately 20 to 100 Angstroms (Macelwee et al.; column 3, lines 39-41).

Regarding claim 3, the combined device shows the CVD oxide layer (Furukawa et al.; 14) is formed of a material of silicon oxide.

Regarding claim 5, the combined device shows growing a thermal oxide layer (Macelwee et al.; 32) using oxygen (Macelwee et al.; column 3, lines 36-41).

Regarding claim 6, the combined device shows growing a thermal oxide layer (Macelwee et al.; 32) having a temperature of approximately 750^0C to 1000^0C (Macelwee et al.; column 3, lines 36-41).

Regarding claim 7, the combined device shows growing a thermal oxide layer (Macelwee et al.; 32) having a temperature of approximately 750^0C to 1000^0C (Macelwee et al.; column 3, lines 36-41).

The combined device differs from the claimed invention by not showing forming a CVD oxide layer having a temperature of approximately 700^0C to 850^0C. It would have been obvious to one having ordinary skill in the art at the time the invention was made for forming a CVD oxide layer having a temperature of approximately 700^0C to 850^0C in order to improve the quality of the thermal oxide layer. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 8, the combined device teaches the surface of the semiconductor substrate comprises a bottom and a sidewall of a trench (Furukawa et al.; figures 2A-G) formed by etching the substrate to a predetermined depth; and wherein the thermal oxide (Macelwee et al.; 32) is formed to a thickness of approximately 20 to 100 Angstroms (Macelwee et al.; column 3, lines 39-41).

The combined device differs in not showing the CVD oxide layer is formed to a thickness of approximately 50 Angstroms to 400 Angstroms. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the CVC oxide layer is formed to a thickness of approximately 50 Angstroms to 400 Angstroms in order to increase the protection for the lower layer. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 9, the combined device shows the CVD oxide layer (Furukawa et al.; 14) is formed of a material of silicon oxide.

3. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Macelwee et al. and Furukawa et al. in view of Maeda, and further in view of US Patent No. 5,994,201 to Lee.

Regarding claim 4, the disclosures of Macelwee et al., Furukawa et al. and Maeda are discussed as applied to claims 1-3 and 5-9 above.

The combined device differs from the claimed invention by not showing forming another material layer on the CVD oxide layer. However, Lee (figures 2A-F) teaches forming another CVD polysilicon layer (208) on the CVD oxide layer (206). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Lee into the method taught by Macelwee et al., Furukawa et al. and Maeda in order to improve the conductivity of the device.

4. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Macelwee et al., Furukawa et al. in view of Maeda, and further in view of US Patent No. 6,074917 to Chang et al.

Regarding claim 10, the disclosures of Macelwee et al., Furukawa et al. and Maeda are discussed as applied to claims 1-3 and 5-9 above.

The combined device shows growing a thermal oxide layer (Macelwee et al.; 32) using oxygen at a temperature of approximately 750^0C to 1000^0C (Macelwee et al.; column 3, lines 36-41).

The combined device differs from the claimed invention by not showing forming oxide layer using N_2O and SiH_4 as source gases at a temperature of approximately 700^0C to 850^0C. However, Chang et al. (abstract) teach forming oxide layer using N_2O and SiH_4 as source gases at a temperature from about 600^0C to 850^0C. Therefore, it would have been obvious to one

having ordinary skill in the art at the time the invention was made to incorporate the teaching of Chang et al. into the device taught by Macelwee et al., Furukawa et al. and Maeda in order to provide high quality of the oxide layer.

5. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Macelwee et al. and Furukawa et al. in view of Maeda, and further in view of US Patent No. 6,180,493 to Chu.

The disclosures of Macelwee et al., Furukawa et al. and Maeda are discussed as applied to claims 1-3 and 5-9 above.

The combined device differs in not showing forming a nitride liner layer on the oxide layer. However, Chu (figures 2A-G) teaches forming a nitride liner layer (214) on the oxide layer (212). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Chu into the device taught by Macelwee et al., Furukawa et al. and Maeda in order to prevent the oxidation on the sidewalls of the trench.

The combined device differs in not showing forming a nitride line layer having a thickness of approximately 30 Angstroms to 100 Angstroms. It would have been obvious to one having ordinary skill in the art at the time the invention was made for forming a nitride line layer having a thickness of approximately 30 Angstroms to 100 Angstroms in order to prevent the oxidation on the sidewalls of the trench. Further, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

The combined device differs in not showing forming a trench filling layer having a thickness of approximately 3000 Angstroms to 10,000 Angstroms. It would have been obvious to one having ordinary skill in the art at the time the invention was made forming a trench filling layer having a thickness of approximately 3000 Angstroms to 10,000 Angstroms in order to improve the trench isolation structure capability and increase the component capability. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

6. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 4,804,633 to Macelwee et al. in view of US Patent No. 6,231,673 to Maeda and US Patent No. 5,837,612 to Ajuria et al.

Regarding claim 12, Macelwee et al. (figure 4) teach a method for forming an oxide layer having a first thickness (the thickness of layer [30] and [32] is about 3100 angstroms) in an integrated circuit device process, comprising:

forming the pad oxide layer (thermal oxide [32]) having a second thickness (thickness of layer [32] is about 100 angstroms) thinner than the first thickness using a thermal oxidation method on a surface of a semiconductor substrate (10); and

forming an oxide layer (30) having a third thickness (thickness of layer [30] is about 3000 angstroms) substantially equal to a difference between the first thickness (3100 angstroms) and the second directly thickness (100 angstroms) on the thermal oxide layer (32).

Macelwee et al. differ from the claimed invention by not showing forming a CVD oxide layer. It would have been obvious to one having ordinary skill in the art at the time the invention was made for forming a CVD oxide layer since it is a well-known method.

The combined device differs in not showing forming a thermal oxide layer and a CVD oxide layer in the same CVD apparatus. However, Maeda (figure 25) teaches conducting processing such as heat treatment, thermal oxidation, and CVD processing (column 15, lines 51-55), a single apparatus, which reads on a CVD apparatus. It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Maeda into the device taught by Macelwee et al. in order to reduce the processing time and contamination.

The combined device differs from the claimed invention by not showing single crystalline silicon substrate. However, Ajuria et al. teach single crystalline silicon substrate. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Ajuria et al. into the device taught by Macelwee et al. and Maeda in order to provide a low resistivity of the device.

The combined device differs from the claimed invention by not showing a thickness of the single crystalline silicon substrate about 8.8 Angstroms to 44 Angstroms. It would have been obvious to one having ordinary skill in the art at the time the invention was made for a thickness of the single crystalline silicon substrate about 8.8 Angstroms to 44 Angstroms in order to provide a low resistivity of the device. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 13, the combined device shows growing a thermal oxide layer (Macelwee et al.; 32) having a temperature of approximately 750^0C to 1000^0C (Macelwee et al.; column 3, lines 36-41).

The combined device differs from the claimed invention by not showing forming a CVD oxide layer having a temperature of approximately 700^0C to 850^0C. It would have been obvious to one having ordinary skill in the art at the time the invention was made for forming a CVD oxide layer having a temperature of approximately 700^0C to 850^0C in order to improve the quality of the thermal oxide layer. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

7. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Macelwee et al. and Maeda in view of Ajuria et al., and further in view of US Patent No. 6,074917 to Chang et al.

Regarding claim 14, the disclosures of Macelwee et al., Maeda and Ajuria et al. are discussed as applied to claims 12-13 above.

The combined device shows growing a thermal oxide layer (Macelwee et al.; 32) using oxygen (Macelwee et al.; column 3, lines 36-41) at a temperature of approximately 750^0C to 1000^0C (Macelwee et al.; column 3, lines 36-41).

The combined device differs from the claimed invention by not showing forming oxide layer using N_2O and SiH_4 as source gases at a temperature of approximately 700^0C to 850^0C. However, Chang et al. (abstract) teach forming oxide layer using N_2O and SiH_4 as source gases

at a temperature from about 600^0C to 850^0C. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Chang et al. into the device taught by Macelwee et al., Maeda and Ajuria et al. in order to provide high quality of the oxide layer.

8. Claims 15, 17, 18, 22, 24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,140,208 to Agahi et al. in view of US Patent No. 6,231,673 to Maeda and US Patent No. 5,837,612 to Ajuria et al.

Regarding claims 15 and 22, Agahi (figures 5-6) teaches a method of forming a layer for an integrated circuit device, comprising:

forming a trench (17) in a single silicon substrate (10) by etching;

forming an oxide layer of a double layer (20, 23) structure with a first thickness (thickness of layer [20] and [23] is about 100 to 500 Angstroms) on a surface of the trench (17);

forming a nitride liner layer (43) on the oxide layer (20, 23), wherein forming the oxide layer comprises:

forming a thermal oxide layer (23) having a second thickness (thickness of layer [23] is about 50 to 200 Angstroms) on the trench (17);

forming a conformal liner material layer (20) having a third thickness (thickness of layer [20] is about 50 to 300 Angstroms) substantially equal to a difference between the first thickness (100 to 500 Angstroms) and the second thickness (50 to 200 Angstroms) directly on the thermal oxide layer (20); and

Agahi et al. differ from the claimed invention by not showing forming a CVD conformal liner material layer. Agahi et al. is silent with respect to how a conformal liner material layer is formed. One having ordinary skill in the art would have been required to select a known method of depositing. It would have been obvious to select CVD, since it is a well-known method.

Agahi et al. differ from the claimed invention by not showing the thermal oxide layer, the conformal liner material layer, and the nitride liner layer are formed in the same chemical vapor deposition (CVD) apparatus. However, Maeda (figure 25) teaches conducting processing such as heat treatment, thermal oxidation, and CVD processing (column 15, lines 51-55), a single apparatus, which reads on a CVD apparatus. It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Maeda into the method taught by Agahi et al. in order to reduce the processing time and contamination.

The combined device differs from the claimed invention by not showing single crystalline silicon substrate. However, Ajuria et al. teach single crystalline silicon substrate. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Ajuria et al. into the device taught by Agahi et al. and Maeda in order to provide a low resistivity of the device.

The combined device differs from the claimed invention by not showing a thickness of the single crystalline silicon substrate about 8.8 Angstroms to 44 Angstroms. It would have been obvious to one having ordinary skill in the art at the time the invention was made for a thickness of the single crystalline silicon substrate about 8.8 Angstroms to 44 Angstroms in order to provide a low resistivity of the device. Furthermore, it has been held that where the general

conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

The combined device differs form the claimed invention by not showing the thickness of the thermal oxide layer about 20 Angstroms to 100 Angstroms. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the thickness of the thermal oxide layer about 20 Angstroms to 100 Angstroms in order to provide a high dielectric strength of the thermal oxide layer. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 17, the combined device differs from the claimed invention by not showing the liner material layer having a thickness of 50 Angstroms to 400 Angstroms. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the liner material layer is formed to a thickness of 50 Angstroms to 400 Angstroms in order to prevent the oxidation on the sidewalls of the trench. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 18, the combined device shows the liner material (Agahi et al.; 20) is made of silicon dioxide.

Regarding claim 24, the combined device differs from the claimed invention by not showing the liner material layer having a thickness of 50 Angstroms to 400 Angstroms. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the liner material layer is formed to a thickness of 50 Angstroms to 400 Angstroms in order to

prevent the oxidation on the sidewalls of the trench. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 26, the combined device shows the liner material (Agahi et al.; 20) is made of silicon oxide.

9. Claims 20, 21 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Agahi et al. and Maeda in view of Ajuria et al., and further in view of US Patent No. 4,804,633 to Macelwee et al. and US Patent No. 6,074917 to Chang et al.

Regarding claims 20 and 25, the disclosures of Agahi et al., Maeda and Ajuria et al. are discussed as applied to claims 15, 17 and 18 above.

The combined device differs from the claimed invention by not showing the thermal oxide layer is formed using oxygen at a temperature of approximately 750^0C to 1000^0C. However, Macelwee et al. teach the thermal oxide layer (32) using oxygen at a temperature of approximately 1000^0C (column 3, lines 36-41). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Macelwee et al. into the device taught by Agahi et al., Maeda and Ajuria et al. in order to improve the insulating breakdown resistance of the thermal oxide layer.

The combined device differs from the claimed invention by not showing forming oxide layer using N_2O and SiH_4 as source gases at a temperature of approximately 700^0C to 850^0C. However, Chang et al. (abstract) teach forming oxide layer using N_2O and SiH_4 as source gases at a temperature from about 600^0C to 850^0C. Therefore, it would have been obvious to one

having ordinary skill in the art at the time the invention was made to incorporate the teaching of Chang et al. into the device taught by Agahi et al., Maeda, Ajuria et al. and Macelwee et al. in order to provide high quality of the oxide layer.

Regarding claim 21, the combined device shows forming a trench isolation material (Agahi et al.; 47) on the nitride liner layer (Agahi et al.; 43) to fill the trench (Agahi et al.; 17) in the same CVC apparatus.

Response to Arguments

Applicant's arguments with respect to claims 1-15, 17-18, 20-22 and 24-26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D. Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
February 3, 2005

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